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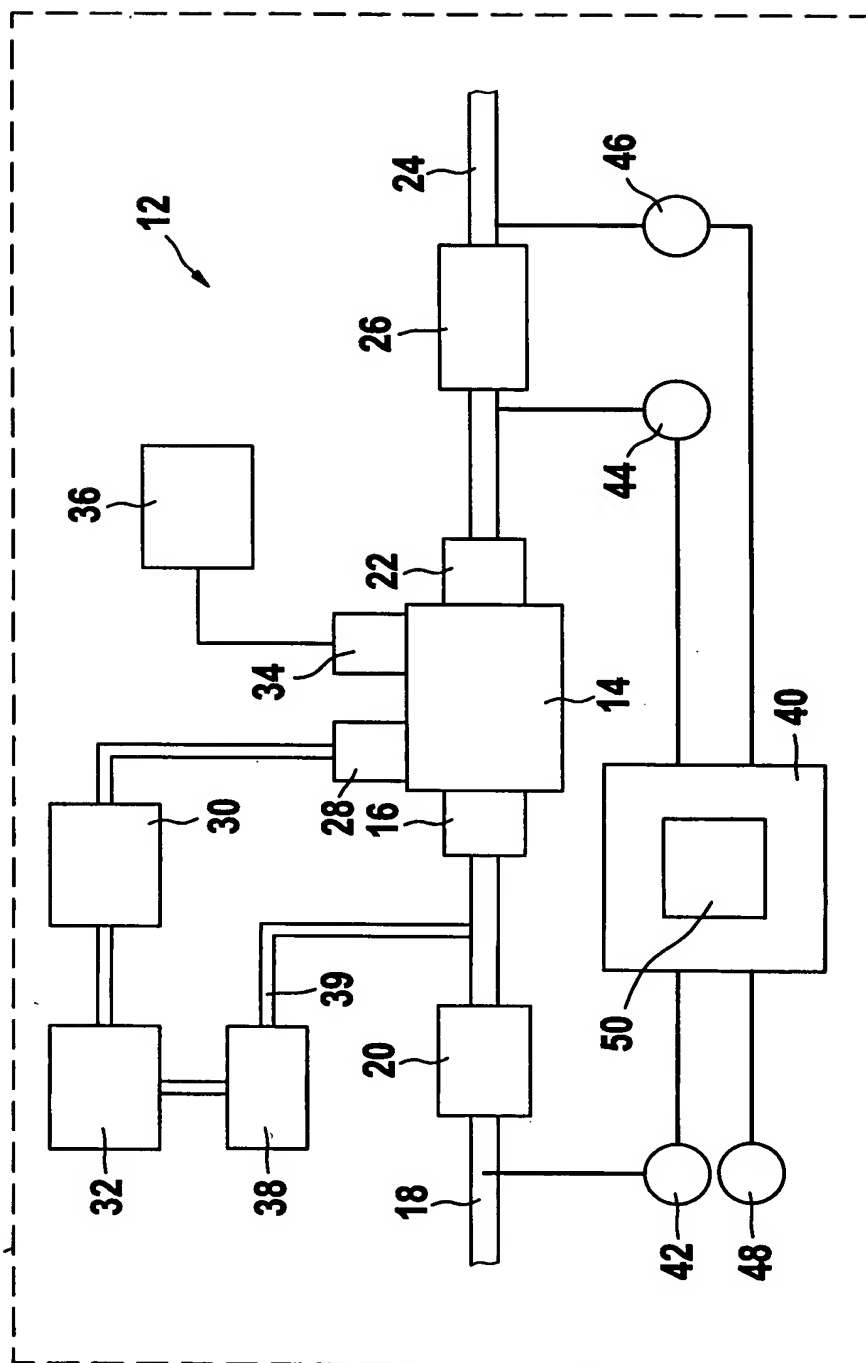


Fig. 2

The diagram illustrates a multi-channel signal processing system, likely for seismic data, consisting of three parallel channels (S1, S2, S3) and a common output stage.

Channels:

- Channel S1:** Input **S1** (in a circle) passes through delay **D-S1** to **FID S1**. **FID S1** outputs to a register **REC-S1** containing **SB-S1**, **IB-S1**, **CB-S1**, **CVA-S1**, and **CVB-S1**. **REC-S1** is connected to **CALC**, which also receives **OC** and **CVB** inputs. **CALC** outputs to a register **PREP** containing **Min**, **CVA-S1**, **CVB-S1**, **CVA-S2**, **CVB-S2**, **CVA-S3**, **CVB-S3**, **CVC**, and **CVD**.
- Channel S2:** Input **S2** (in a circle) passes through delay **D-S2** to **FID S2**. **FID S2** outputs to a register **REC-S2** containing **SB-S2**, **IB-S2**, **CB-S2**, **CVA-S2**, and **CVB-S2**. **REC-S2** is connected to **CALC**, which also receives **OC** and **CVB** inputs. **CALC** outputs to the **PREP** register.
- Channel S3:** Input **S3** (in a circle) passes through delay **D-S3** to **FID S3**. **FID S3** outputs to a register **REC-S3** containing **SB-S3**, **IB-S3**, **CB-S3**, **CVA-S3**, and **CVB-S3**. **REC-S3** is connected to **CALC**, which also receives **OC** and **CVB** inputs. **CALC** outputs to the **PREP** register.

Common Output Stage:

- The **PREP** register outputs to a block **54**.
- Block **54** outputs to a block **52**.
- Block **52** outputs to a block **50**.
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